

Forward Error Correction Acceleration Proposal for TigerSHARC

■ What:

- ☐ Add three new instructions to reduce TigerSHARC Clock cycle requirements

- TMAX
- ACS
- PERMUTE

■ Why:

- ☐ Competition

- DSP
- ASIC

- ☐ Customer channel capacity requirements



TigerSHARC FEC Benchmarks

Algorithm	TS001		TMAX ^(*)		ACS		PERMUTE	
	Cycles	Efficiency	Cycles	Efficiency	Cycles	Efficiency	Cycles	Efficiency
8-Bit Viterbi	N*91	6.5%			N*67	6.5%		
	N*23				N*23			
	Butterfly	61.5%			N*28	85.7%		
	Scale	N/A			N*9	N/A		
	Trace	N/A			N*7	N/A		
16-Bit Viterbi	N*128				N*80			
	N*17	17.6%			N*17	17.6%		
	Butterfly	61.5%			N*36	85.7%		
	Scale	N/A			N*7	N/A		
	Trace	N/A						
Turbo Decoder	N*45:50		N*15:50		N*11:50		N*10:75	
	N*0:50	57.1%	N*0:50	57.1%	N*0:50	57.1%	N*0:50	57.1%
	Gamma							
	Butterfly	19.2%	N*8:50	55.2%	N*1:50	66.7%	N*4:50	66.7%
	Trace							
EXTRA96	N*20:50	23.0%	N*6:50	72.5%	N*6:50	72.5%	N*5:75	82.2%

Table 1. Iterative TigerSHARC Channel Decoder Performance Resulting from New Instructions

* TMAX improves SNR by 0.5 dB.

** 52.5% efficiency if you include scaling in with Butterfly calculation.

Acceleration Performance

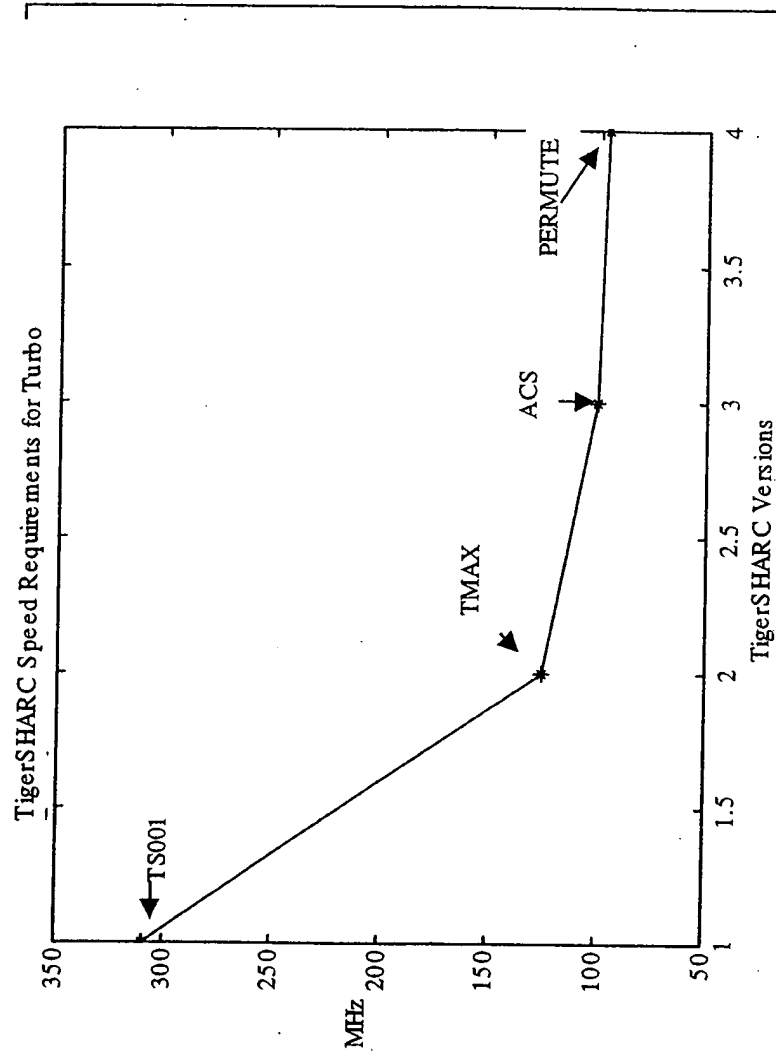


Figure 1. TigerSHARC-MIPs requirement to handle 1 384kps data channel for 4 versions.
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MIPS Required for Transmit and Receive Functions for a 12.8kbps Voice Channel

A MIP = 1 million machine cycles in one second

User Data Rate	Viterbi Decoder K=9, R=1/3	All Other Functions	Total
12.8 kbps	1.2	1.5	2.7

Viterbi decoder in assembler, all other algorithms in C

MIPS Required for Transmit and Receive Functions for a 384kbps Data Channel

A MIPS = 1 million machine cycles in one second

User Data Rate	Turbo Decoder K=4, R=1/3, 8 iterations	All Other Functions	Total
384kbps	96.4	28.6	125

- Turbo decoder (Max log MAP) done in assembler
- Assumes the MIPS for the interleaver in the decoder can be hidden
- All other functions in C

TigerSHARC Viterbi Performance

Algorithm (K=9, R=1/3)	Cycle Count n = # of bits	Cycles/ACS
8 Bit Viterbi	$n * 91 + 20$	0.50
16 Bit Viterbi	$n * 128 + 21$	0.75

- Viterbi Butterflies executed using SIMD in both compute blocks
- VMAX instruction compares, selects and records traceback bit with single cycle throughput.
- ADD/SUB instruction results in quick metric calculation

TigerSHARC Trellis Butterflies (8)

```
sR9:8   = R1:0   + R29:28, bR1:0   = R1:0   - R29:28;;  
sR29:28 = R13:12 + R29:28, bR25:24 = R13:12 - R29:28;;  
  
sR11:8  = MERGE R9:8 , R1:0 ;;  
sR27:24 = MERGE R25:24 , R29:28;;  
  
sR9:8   = VMAX(R25:24, R9:8   );;  
sR11:10 = VMAX(R27:26, R11:10 );;
```

q[K11 += 4] = XR11:8;;
q[K11 + 28] = YR11:8;;



Can be hidden in next add

TigerSHARC Turbo Decoder Performance

Algorithm	Cycle Count / Decode Block n = # of bits	Cycles/ACS
Max Log MAP (K=4, R=1/3)	$(N * 15.75) + 57$	0.5

- SIMD Instructions execute Forward and Reverse Trellis in parallel
 - Alpha metric calculated in Compute Block X
 - Beta metric calculated in Compute Block Y
- MAX instruction compares and selects updated metric and extrinsic approximation.
- ADD/SUB instruction results in quick metric calculation

